Amendments to the Claims

1. (Currently amended) A process for forming a capacitor structure comprising:

forming a BPSG insulating layer over a semiconductor substrate;

forming a container in said insulating layer;

forming an HSG polysilicon lower electrode layer along an inner surface of said container, wherein said HSG polysilicon lower electrode layer is formed so as to extend beyond said inner surface of said container, and said HSG polysilicon lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the insulating layer;

forming a silicon nitride dielectric layer characterized by a given degree of uniformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of silicon nitride over HSG polysilicon and BPSG, and

said thickness of said silicon nitride dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said HSG polysilicon lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

2. (Canceled).

3. (Original) A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend along an upper surface of said insulating layer.

4. (Original) A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend from said inner surface in the direction of an upper surface of said insulating layer along an extension of said container.

5. (Original) A process for forming a capacitor structure as claimed in claim 1 wherein said lower electrode layer is formed so as to extend along an upper surface of said insulating layer and from said inner surface in the direction of said upper surface of said insulating layer along an extension of said container.

6. (Original) A process for forming a capacitor structure as claimed in claim 1 wherein said dielectric layer is formed on said lower electrode layer.

7. (Currently amended) A process for forming a capacitor structure comprising:

forming a BPSG insulating layer over a semiconductor substrate;

forming a container in said insulating layer;

forming an HSG polysilicon lower electrode layer along an inner surface of said container, wherein said HSG polysilicon lower electrode layer is formed so as to extend beyond said inner surface of said container, and said HSG polysilicon lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the BPSG insulating layer;

forming a silicon nitride dielectric layer less than about 50 angstroms in thickness and characterized by a given degree of uniformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of less than 50 angstrom thick silicon nitride over HSG polysilicon and BPSG, and

said thickness of said silicon nitride dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said HSG polysilicon lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

8. (Currently amended) A process for forming a capacitor structure comprising:

forming an insulating layer over a semiconductor substrate;

forming a container in said insulating layer;

forming a lower electrode layer along an inner surface of said container, wherein said lower electrode layer is formed so as to extend beyond said inner surface of said container, and said lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the insulating layer;

forming a dielectric layer characterized by a given degree of uniformity over said lower electrode layer and an upper surface of said insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of a dielectric layer over an electrode layer and an insulating layer, and

said thickness of said dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.

9. (Currently amended) A process for forming a memory cell comprising:

forming a semiconductor structure defining a transistor and a pair of transistor node locations in a semiconductor substrate;

forming a BPSG insulating layer over said semiconductor substrate;

forming a container in said insulating layer over one of said transistor node locations;

forming an HSG polysilicon lower electrode layer along an inner surface of said container, wherein said HSG polysilicon lower electrode layer is formed so as to extend beyond said inner surface of said container, and said HSG polysilicon lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the BPSG insulating layer;

forming a silicon nitride dielectric layer characterized by a given degree of uniformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer; and

forming an upper electrode layer over said reoxidized layer.

10. (Currently amended) A process for forming a memory cell comprising:

forming a semiconductor structure defining a transistor and a pair of transistor node locations in a semiconductor substrate;

forming a BPSG insulating layer over said semiconductor substrate;

forming a container in said insulating layer over one of said transistor node locations;

forming an HSG polysilicon lower electrode layer along an inner surface of said container, wherein said HSG polysilicon lower electrode layer is formed so as to extend beyond said inner surface of said container, and said HSG polysilicon lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the BPSG insulating layer;

forming a silicon nitride dielectric layer less than about 50 angstroms in thickness and characterized by a given degree of uniformity over said HSG polysilicon lower electrode layer and an upper surface of said BPSG insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said HSG lower electrode

layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said silicon nitride dielectric layer; and

forming an upper electrode layer over said reoxidized layer.

11. (Currently amended) A process for forming a memory cell comprising:

forming a semiconductor structure defining a transistor and a pair of transistor node locations in a semiconductor substrate;

forming an insulating layer over said semiconductor substrate;

forming a container in said insulating layer over one of said transistor node locations;

forming a lower electrode layer along an inner surface of said container, wherein said lower electrode layer is formed so as to extend beyond said inner surface of said container, and said lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the insulating layer;

forming a dielectric layer characterized by a given degree of uniformity over said lower electrode layer and an upper surface of said insulating layer through an atomic layer deposition process where a silicon-containing precursor is chemisorbed over a surface of said lower electrode layer and a nitrogen-containing precursor is reacted with said chemisorbed silicon-containing precursor to form said dielectric layer such that

said given degree of uniformity exceeds a degree of uniformity attributable to LPCVD nucleation incubation of a dielectric layer over an electrode layer and an insulating layer, and

said thickness of said dielectric layer is sufficient to prevent oxidation punch-through from a reoxidized layer formed over said dielectric layer to said lower electrode layer; and

forming an upper electrode layer over said reoxidized layer.